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INTERNATIONAL DATA SCIENCES, INC.
ADVANCED TECHNIQUES IN DATA COMMUNICATIONS

MANUAL OF OPERATION

MODEL 3000E

DATA TRANSMISSION TEST SET

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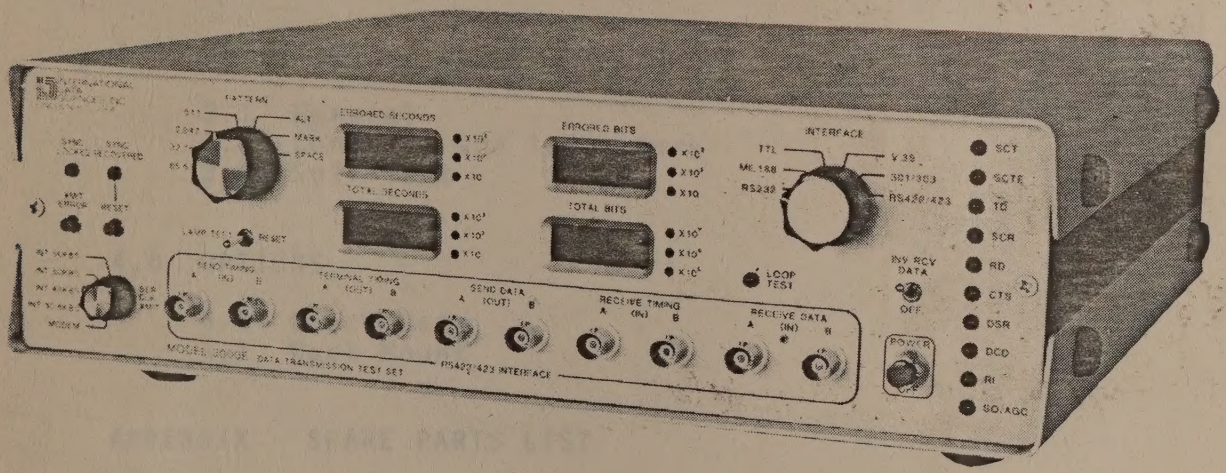

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1.0 INTRODUCTION

1.1 General

The IDS Model 3000E Data Transmission Test Set, shown in Figure 1-1, performs high-speed bit error rate testing of data communication channels at operating speeds up to 10 megabits per second.

The Model 3000E, henceforth referred to as the Data Test Set, is capable of generating and transmitting seven repeating pseudo-random bit patterns. Errors can be injected into the pattern for comparison with a true replica of the transmitted pattern in the units' receiver section. A unique sync detect circuit allows the data test set to detect the loss of synchronization and subsequently recover it in less than 100 bits.

The following sections of this manual provide information on the installation and operation of the Data Test Set.

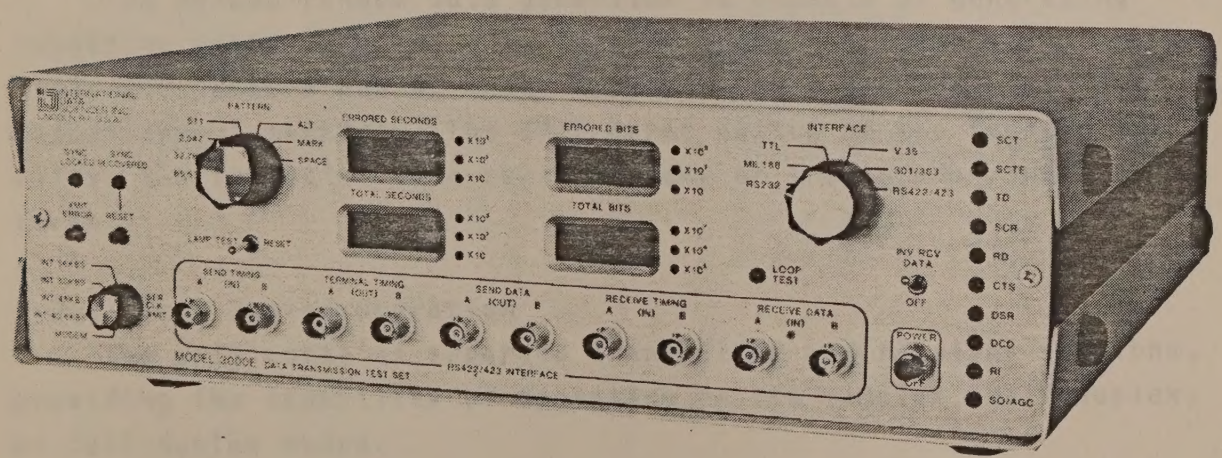

Figure 1-1. IDS Model 3000E Data Transmission Test Set

1.2 Features

Functional features of the Data Test Set are described in the following paragraphs.

1.2.1 Interface

The Data Test Set is compatible with the following interfaces: RS-232, MIL-188, TTL, V.35, 301/303, and RS-422/423. These six interfaces are switch selectable, including RS-449 which is accessed through a 37-pin rear panel connector and selected on the front panel with RS-422/423. Interface modes are selected through internal strapping on the interface board (see Section 2.7).

1.2.2 Clock Generator

The Data Test Set offers four internally generated data rates of 40.8, 48, 50, and 56 Kilobits per second. The standard data rates of 40.8 and 48 Kbps can be replaced by any frequency required by the user. The Data Test Set is capable of operating with external timing of up to 10 Megabits per second.

1.2.3 Data Generator

The pseudo-random data generator is capable of generating repeating patterns of 65,535; 32,767; 2,047; and 511 bits. An alternate pattern and a steady mark and space are included for miscellaneous testing. The XMIT Error switch on the front panel allows the injection of errors into any of the pseudo-random patterns.

1.2.4 Full Duplex Operation

The unit contains separate transmitter and receiver sections, providing the capability of operating in the simplex, half-duplex, or full-duplex modes.

1.3 Typical Application

In this application, two Model 3000E Data Test Sets are being used to conduct bit error rate tests on each end of a communications channel.

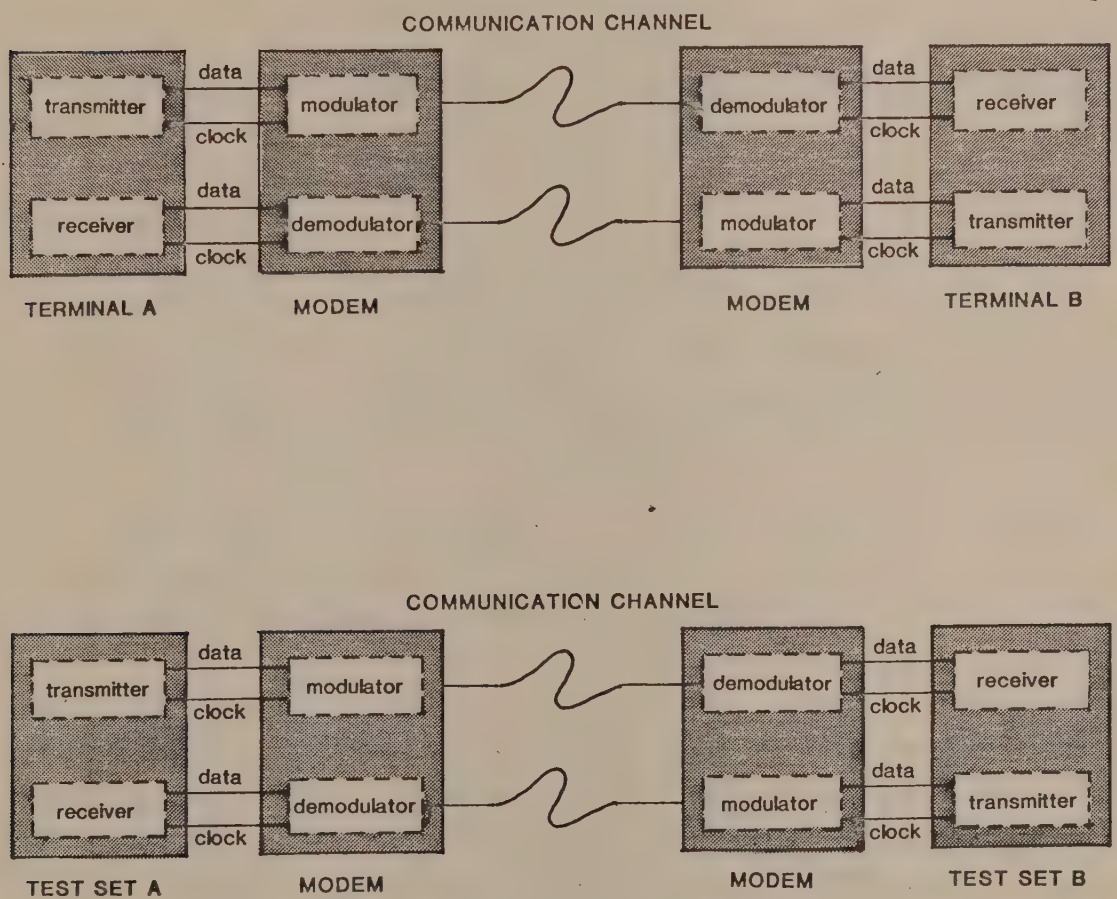

Figure 1-2. Typical Application

1.4 Technical Specifications

1.4.1 Dimensions

Height: 4¼ inches (10.6 cm)
Width: 14½ inches (47.1 cm)
Depth: 14¼ inches (36.2 cm)

1.4.2 Weight

The Data Test Set weighs approximately 15 pounds, 4 ounces (6.8 Kg), uncrated.

1.4.3 Primary Power

The Data Test Set is switch selectable for 115 VAC, 60 Hz ±10% or 230 VAC, 50 Hz ±10% power input. Internal protection is provided by a 3/4 Amp, Slow Blow fuse and a 3/8 Amp, Slow Blow fuse, respectively. Power consumption is approximately 40.5 watts during normal operation and 46.6 watts during Lamp Test.

1.4.4 Environmental Conditions

Operating Temperature: 0^{o} - 50^{o}C.
Relative Humidity: 90%, non-condensing.

1.4.5 Interface

There are six standard interfaces on the data test set. All are switch selectable and accessed through separate connectors. Five 25-pin "D" connectors are used for RS-232, MIL-188, TTL, V.35, and 301/303 interfaces. A single 37-pin "D" connector is used for the RS-422/423 and RS-449 interfaces.

1.5 Options

Table 1-1 lists and describes options available for use with the Data Test Set. These options are further described in Section 4.0.

TABLE 1-1. OPTIONS

Option	Description
Rack Mount	Allows Data Test Set to be mounted in a standard 19-inch cabinet.
Data Rate	Two standard data rates of 40.8 and 48 Kbps can be substituted with any data rate required by the user (up to 10 Mbps).

2.0 INSTALLATION

2.1 General

This section provides information to satisfy general mechanical and electrical installation and strapping requirements. Field service personnel should become familiar with all installation procedures before attempting to install the test set. Upon completion of all installation requirements, refer to Section 3.0 for power-up and operation/test procedures.

2.2 Site Preparation

The installation area should be clean, well lighted, and free from extremes of temperature, humidity, appreciable shock, and vibration. A grounded AC outlet capable of furnishing primary power as specified in paragraph 1.4.3 should be located within 7½ feet of the installation area.

2.3 Unpacking and Inspection

Before unpacking the test set, inspect the packing container for unusual damage. Then unpack the unit and inspect it for external damage such as scratches or dents and broken controls, indicators, and connectors. If physical damage is present, retain the packing material and contact the carrier immediately. Each test set has been thoroughly inspected prior to shipment.

2.4 Tools/Equipment/Materials Required

No special tools or equipment are required to install the test set. Any standard field service tool kit can be used.

2.5 Mechanical Installation

2.5.1 Desktop

The Data Test Set is a free-standing unit equipped with plastic feet and a metal bale. Use of the bale tilts the front of the Data Test Set upward, providing a better view of the display and better access to the front panel controls.

2.5.2 Rack Mount

An optional rack mount adapter is available for mounting the Data Test Set in a standard 19-inch cabinet. This option is further described in Section 4.0.

2.6 Electrical Installation

2.6.1 AC Power Cord

AC power is supplied to the Data Test Set through a removable 7½-foot line cord with a grounded 3-wire plug. The line cord mates with a receptacle at the rear of the unit (see Figure 2-1). Power requirements are specified in paragraph 1.3.3.

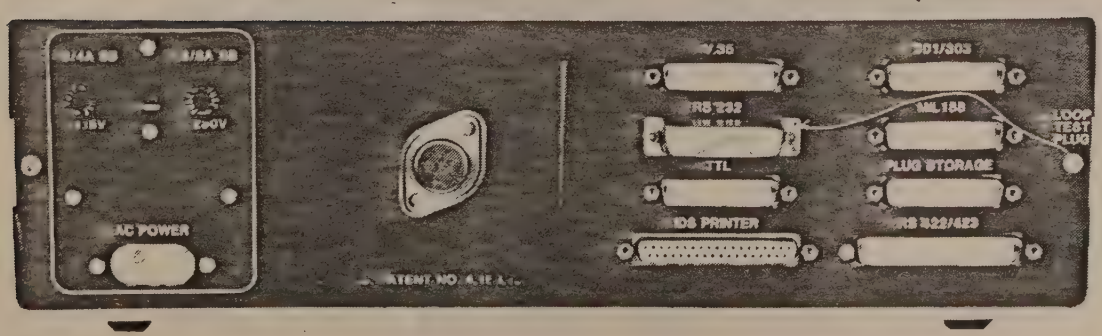

Figure 2-1. Rear Panel Connectors

2.6.2 Interface

Standard interfaces for the Data Test Set include RS-232, MIL-188, V.35, 301/303, RS-422/423, and TTL. These interfaces are described in detail in the following paragraphs.

2.6.2.1 EIA RS-232 Interface. A male 25-pin "D" type connector provides the interface for connecting the Data Test Set to the data communications equipment. This interface conforms to the EIA RS-232-C Standard and the CCITT V.24 Standard. Table 2-1 lists and describes the function and direction of each pin assignment.

The Data Test Set is connected to the data communications equipment via a six-foot standard 25-conductor EIA interface cable supplied with the unit.

Electrical specifications for EIA interface signals are as follows:

a. Interface Output Drivers:

Binary One - -6V ±0.5V.
Binary Zero - +6V ±0.5v.
Impedance - Less than 100 ohms for data and clock signals.
Less than 1000 ohms for control signals.
Control Signals On, Space - +12V ±1V.
Control Signals Off, Mark - -12V ±1V.
Protection - All outputs are protected against damage caused by accidental shorting up to ±25V.

b. Interface Input Receivers:

Binary One - -2V to -25V.
Binary Zero - +2V to +25V.
Impedance - 3000 ohms to 7000 ohms.
Noise Immunity - ±2V with hysteresis.
Protection - ±25 volts without damage to receiver circuits.

TABLE 2-1. EIA/CCITT INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		CIRCUIT		DESCRIPTION
		TO DTE	TO DCE	EIA	CCITT	
1	FG			AA	101	FRAME GROUND - This lead is an electrical equipment frame and power ground.
2	TD		→	BA	103	TRANSMITTED DATA - This lead carries the serial digital data transmitted from the DTE to the DCE.
3	RD	←		BB	104	RECEIVED DATA - This lead carries the serial digital data received at the DTE.
4	RTS		→	CA	105	REQUEST TO SEND - An "ON" condition on this lead is used to enable the local DCE for data transmission.
5	CTS	←		CB	106	CLEAR TO SEND - An "ON" condition on this lead indicates whether or not the DCE is ready to transmit data.
6	DSR	←		CC	107	DATA SET READY - An "ON" condition on this lead indicates that the local DCE is ready to process data and is not in a test, talk, or dial mode.
7	SG			AB	102	SIGNAL GROUND - This lead establishes the common ground reference potential for all circuits except frame ground on Pin 1.
8	DCD	←		CF	109	DATA CARRIER DETECT (Received Line Signal Detector) - This lead indicates that data from the remote location is being received and meets suitable criteria established by the DCE manufacturer.
9	-					Not Used.
10	-					Not Used.
11	-					Not Used.
12	-					Not Used.
13	-					Not Used.
14	-					Not Used.
15	TC	←		DB	114	TRANSMITTER CLOCK - This lead is used to provide the DTE with signal element timing information.
16	-					Not Used.
17	RC	←		DD	115	RECEIVER CLOCK - This lead is used to provide the DTE with received signal element timing information.

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TABLE 2-1. EIA/CCITT INTERFACE DESCRIPTION (continued)

PIN #	MNEMONIC NAME	DIRECTION		CIRCUIT		DESCRIPTION
		TO DTE	TO DCE	EIA	CCITT	
18	-					LOOP SENSE
19	-					Not Used.
20	DTR		→	CD	108.2	DATA TERMINAL READY - An "ON" condition on this lead indicates that the DTE is ready to be connected to the communication channel.
21	SQ	←		CG	110	SIGNAL QUALITY DETECT - This lead is used to indicate whether or not there is a high probability of an error in the received data.
22	RI	←		CE	125	RING INDICATOR - An "ON" condition on this lead indicates that a ringing signal is being received on the communication channel.
23	-					Not Used.
24	(TC)		→	DA	113	EXTERNAL TRANSMITTER CLOCK - This lead is used to provide the transmitting signal converter with signal element timing information.
25	-					Not Used.

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2.6.2.2 MIL-188. A 25-pin "D" type male connector provides the interface for connecting the Data Test Set to the data communications equipment. This interface conforms to MIL-188 Standard. Interface pin assignments are the same as RS-232, described in Table 2-1.

Electrical specifications for the MIL-188 interface are as follows:

Binary One - +6V ±0.5V.
Binary Zero - -6V ±0.5V.
Driver Impedance (Z_{out}) - Less than 100 ohms for data and clocks.
Less than 1000 ohms for control signals.
Receiver Impedance (Z_{in}) - 6000 ohms, minimum.
Receiver Noise Immunity - ±0.6V with hysteresis.
Receiver Protection - ±25V without damage.

2.6.2.3 V.35 Interface. A male 25-pin "D" type connector provides the interface for connecting the Data Test Set to the data communications equipment. Table 2-2 lists and describes the function and direction of each pin assignment.

A six-foot 25-conductor cable, terminated with a female 25-pin EIA connector and a male 34-pin Winchester connector, is provided with the unit. Figure 2-2 shows the wiring configuration between the two connectors.

Electrical Specifications for the CCITT V.35 interface are as follows:

Binary One - Output A negative with respect to output B.
Binary Zero - Output A positive with respect to output B.
Levels - ±1.1V.

TABLE 2-2. V.35 INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		FUNCTION
		TO DTE	TO DCE	
1	FG			FRAME GROUND
2	SD (A)		→	SEND DATA (SIGNAL A)
3	RD (A)	←		RECEIVED DATA (SIGNAL A)
4	SD (B)		→	SEND DATA (SIGNAL B)
5	RD (B)	←		RECEIVED DATA (SIGNAL B)
6	DSR	←		DATA SET READY
7	SG			SIGNAL GROUND
8	RLSD	←		RECEIVED LINE SIGNAL DETECTOR
9	RTS		→	REQUEST TO SEND
10	CTS	←		CLEAR TO SEND
11	-			NOT USED
12	-			NOT USED
13	-			NOT USED
14	SCT (A)	←		SER. CLK. XMIT (SIG. A)
15	SCT (B)	←		SER. CLK. XMIT (SIG. B)
16	SCR (B)	←		SER. CLK. RECEIVE (SIG. B)
17	SCR (A)	←		SER. CLK. RECEIVE (SIG. A)
18	-			LOOP SENSE
19	-			NOT USED
20	DTR		→	DATA TERMINAL READY
21	-			NOT USED
22	RI	←		RING INDICATOR
23	-			NOT USED
24	SCTE (A)		→	SER. CLK. XMIT EXT. (SIG. A)
25	SCTE (B)		→	SER. CLK. XMIT EXT. (SIG. B)

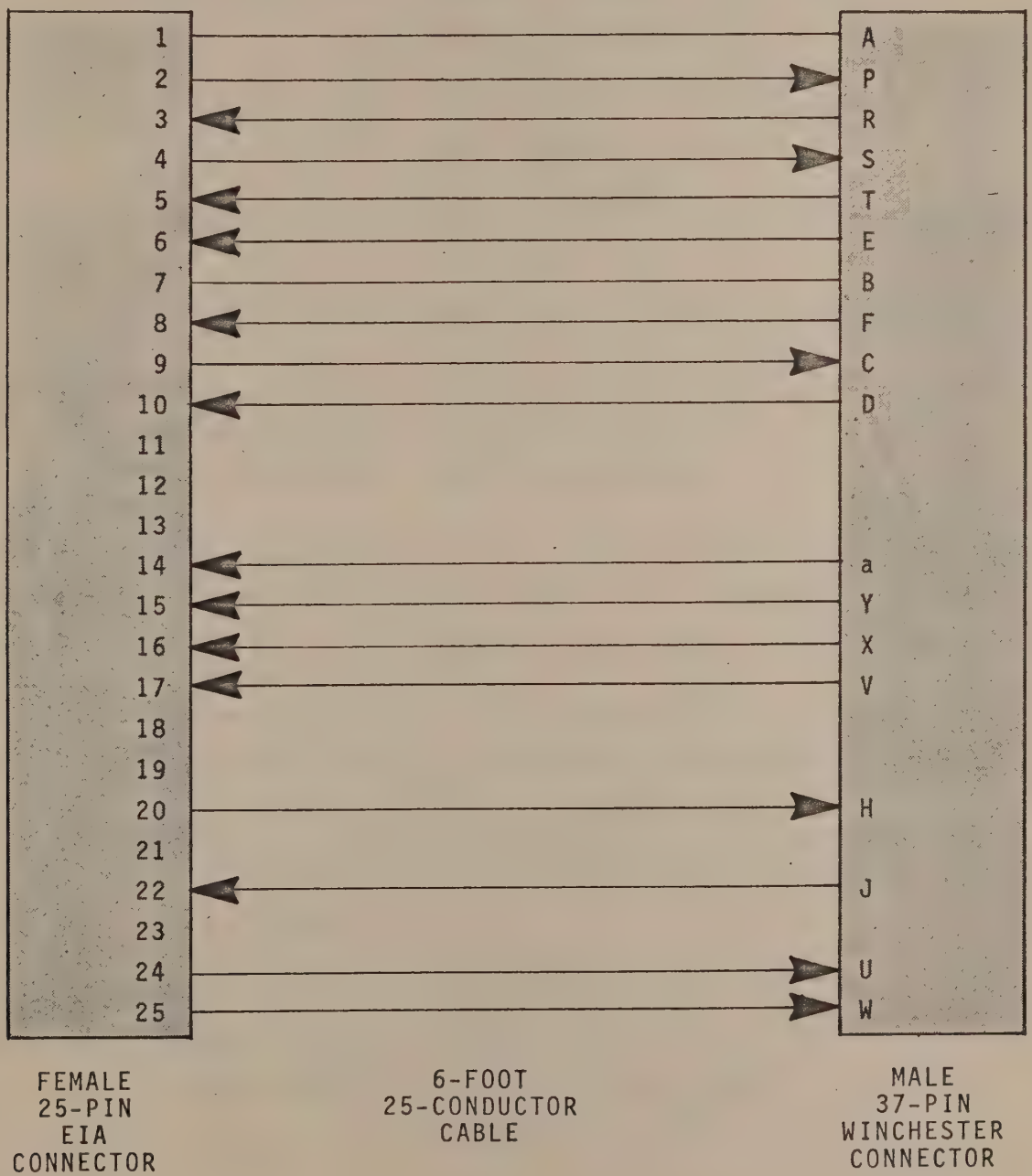


Figure 2-2. V.35 Interface Adaptor Cable

2.6.2.3 V.35 Interface. (continued)

Rise and Fall Time - Greater than 40 nanoseconds when measured between 10% and 90% of waveform rise and fall.

Impedance - 100 ohms ±1% balanced, 150 ohms ±1% with respect to ground with A and B shorted together.

Driver DC Offset - 0V ±0.2V for each output with respect to ground.

Driver Protection - Short circuit protected outputs to ground or to each other.

Receiver Sensitivity - ±10 millivolts, maximum.

Receiver DC Offset - ±0.6V, maximum.

Receiver Protection - ±10V without damage.

2.6.2.4 301/303 Interface. A male 25-pin connector provides the interface for connecting the Data Test Set to the data communications equipment. Table 2-3 lists and describes the function and direction of each pin assignment.

A six-foot 15-conductor cable, terminated with a female 25-pin EIA connector and a male 12-pin Burndy connector is provided to interconnect the Data Test Set to the data interface. Figure 2-3 shows the wiring configuration between the two connectors.

Electrical specifications for the Bell 301/303 current type interface are as follows:

Binary One (Mark), Off - Less than 5 mA.

Binary Zero (Space), On - Greater than 23 mA.

Receiver Impedance (Z_{in}) - 100 ohms ±5%.

Open Circuit - Receiver assumes an Off or Mark Hold condition.

TABLE 2-3. 301/303 INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		FUNCTION
		TO DTE	TO DCE	
1	FG			FRAME GROUND
2	SD		→	SEND DATA
3	RD	←		RECEIVE DATA
4	RS		→	REQUEST TO SEND
5	CS	←		CLEAR TO SEND
6	DSR	←		DATA SET READY
7	SG			SIGNAL GROUND
8	-			NOT USED
9	-			NOT USED
10	-			NOT USED
11	-			NOT USED
12	-			NOT USED
13	-			NOT USED
14	-			NOT USED
15	SCT	←		SERIAL CLOCK TRANSMIT
16	-			NOT USED
17	SCR	←		SERIAL CLOCK RECEIVE
18	-			LOOP SENSE
19	-			NOT USED
20	DTR		→	DATA TERMINAL READY
21	AGC	←		AUTOMATIC GAIN CONTROL
22	RI			RING INDICATOR
23	-			NOT USED
24	SCTE		→	SERIAL CLOCK XMIT EXTERNAL
25	-			NOT USED

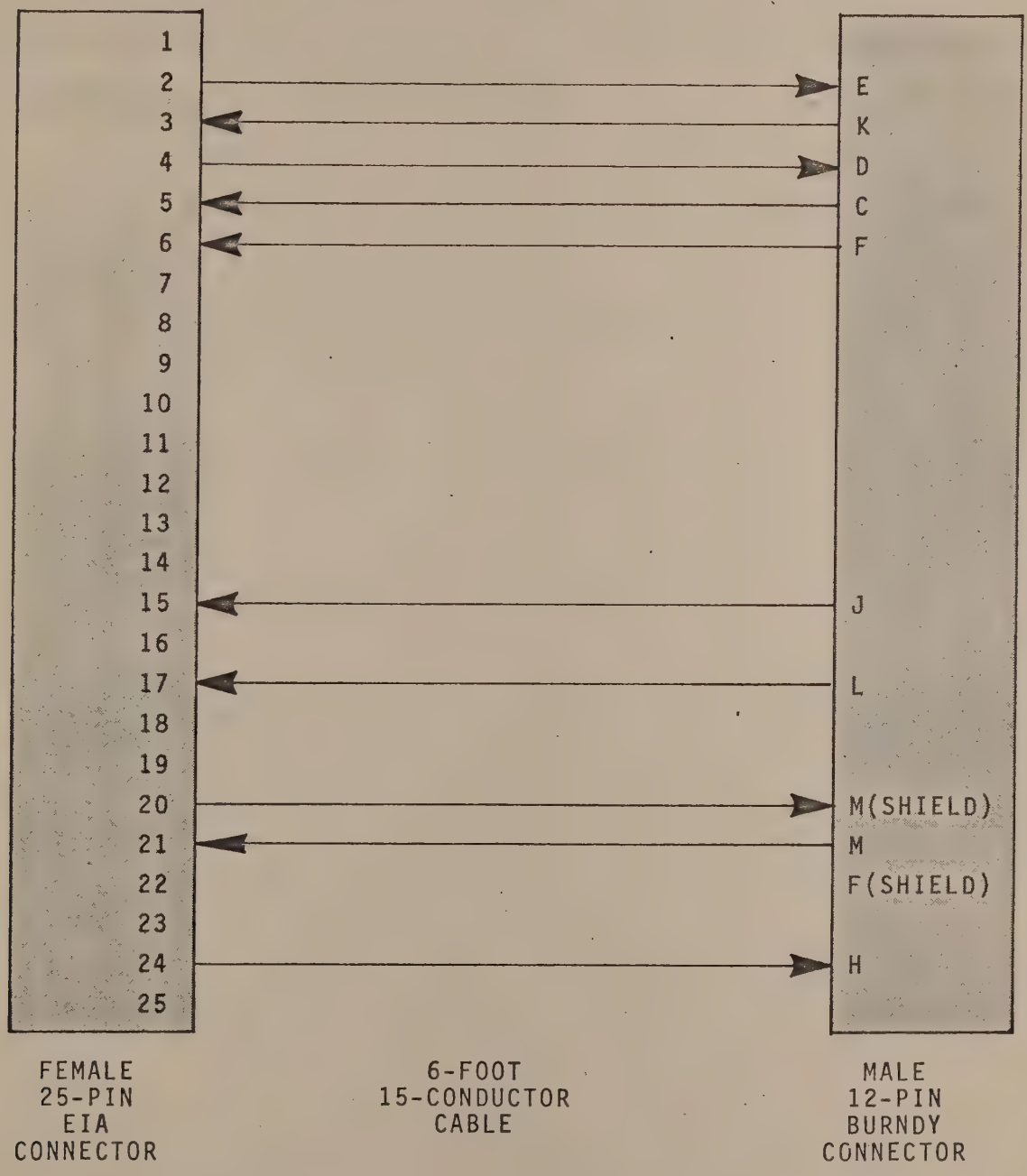


Figure 2-3. 301/303 Interface Adaptor Cable

2.6.2.5 TTL Interface. A male 25-pin "D" type connector provides the interface for connecting the Data Test Set to the data communications equipment. Table 2-4 lists and describes the function and direction of each pin assignment.

A six-foot, standard 25-conductor EIA interface cable is supplied with the unit.

Electrical specifications for the TTL interface are as follows:

Binary One (Driver)	5V ±0.2V.
Binary One (Receiver)	Greater than 1.5V.
Binary Zero (Driver)	0V ±0.7V.
Binary Zero (Receiver)	Less than 1.1V.
Driver Impedance (Z_{out})	125 ohms ±5%.
Driver Protection	Output protected against short circuit to ground.
Receiver Impedance (Z_{in})	Greater than 5.5K ohms.
Receiver Protection	-0.7 to 5.5V.

2.6.2.6 RS-422/423 Interface. A male 37-pin connector provides the interface for connecting the Data Test Set to the data communications equipment. Ten front panel BNC inputs provide optional access to the data and timing signals of this interface. Strapping information for interface options can be found in Section 2.7. Interface pin assignments and signal flow, per RS-422/423 specifications are listed and described in Table 2-5.

A standard six-foot 37-conductor cable, terminated with a male and female "D" type connector, is provided with the unit.

Electrical specifications for the RS-422/423 interface are as follows:

Binary One (Mark), Off	A negative with respect to B.
Binary Zero (Space), On	A positive with respect to B.
Driver Impedance (Z_{out})	100 ohms ±1% balanced.
	50 ohms ±1% single ended.

TABLE 2-4. TTL INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		FUNCTION
		TO DTE	TO DCE	
1	FG			FRAME GROUND
2	TD		→	TRANSMITTED DATA
3	RD	←		RECEIVED DATA
4	RTS		→	REQUEST TO SEND
5	-			NOT USED
6	-			NOT USED
7	SG			SIGNAL GROUND
8	-			NOT USED
9	-			NOT USED
10	-			NOT USED
11	-			NOT USED
12	-			NOT USED
13	-			NOT USED
14	-			NOT USED
15	TC	←		TRANSMITTER CLOCK
16	-			NOT USED
17	RC	←		RECEIVER CLOCK
18	-			LOOP SENSE
19	-			NOT USED
20	DTR		→	DATA TERMINAL READY
21	-			NOT USED
22	-			NOT USED
23	-			NOT USED
24	(TC)		→	EXT. TRANSMITTER CLOCK
25	-			NOT USED

TABLE 2-5. RS-422/423 INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		FUNCTION
		TO DTE	TO DCE	
1				SHIELD
2	-			NOT USED
3	-			NOT USED
4	SD		→	SEND DATA A
5	ST	←		SEND TIMING A
6	RD	←		RECEIVE DATA A
7	RS		→	REQUEST TO SEND A
8	RT	←		RECEIVE TIMING A
9	CS	←		CLEAR TO SEND A
10	-			NOT USED
11	DM	←		DATA MODE A
12	TR		→	TERMINAL READY A
13	RR	←		RECEIVER READY A
14	-			NOT USED
15	IC	←		INCOMING CALL
16	-			NOT USED
17	TT			TERMINAL TIMING A
18	-			NOT USED
19	SG			SIGNAL GROUND
20	RC	←		RECEIVE COMMON
21	-			NOT USED
22	SD		→	SEND DATA B
23	ST	←		SEND TIMING B
24	RD	←		RECEIVE DATA B
25	RS		→	REQUEST TO SEND B
26	RT	←		RECEIVE TIMING B
27	CS	←		CLEAR TO SEND B
28	-			NOT USED
29	DM			DATA MODE B
30	TR		→	TERMINAL READY B
31	RR			RECEIVER READY B
32	-			NOT USED
33	SQ	←		SIGNAL QUALITY
34	-			NOT USED
35	TT		→	TERMINAL TIMING B
36	-			NOT USED
37	SC		→	SEND COMMON

2.6.2.6 RS-422/423 Interface. (continued)

Rise and Fall Time - Greater than 20 nanoseconds when measured between 10% and 90% of rise or fall.

Driver DC Offset - 0V ±0.5V balanced.
0V ±0.25V single ended.

Driver Protection - Outputs short circuit protected to ground or to each other (150 mA maximum).

Receiver Sensitivity - ±200 mv maximum balanced.
±400 mv maximum single ended.

Receiver Impedance (Z_{in}) - 4000 ohm minimum single ended.
2000 ohm minimum single ended.

Receiver DC Offset - ±7V maximum for proper operation.

Receiver Protection - ±15V maximum without damage to receiver circuits.

2.6.2.7 IDS Printer Interface. A female 37-pin connector provides the interface to allow for the interconnection of an IDS Model 2910D Data Test Set Printer. Table 2-6 lists and describes the pin assignments for the printer interface. In a typical application, Model 3000E Data Test Sets perform bit error rate tests (BERT) at each end of a data link while Model 2910D Printers provide an unattended hard-copy record of the results.

TABLE 2-6. IDS PRINTER INTERFACE DESCRIPTION

Pin Number	Signal Name	Signal Flow	Description
1	Not Used		
2	Errored Seconds	To Printer	A negative going pulse for each detected Errored Second.
3	Receive Clock (SCR)	To Printer	A normally low signal which goes high when the receiver clock input to test set is absent.
4	BCD Bit 800	To Printer	BCD data output of either Errored Seconds, Total Seconds, Errored Bits, or Total Bits. The output selected is controlled by printer input commands as described on Pins 26, 27, and 28 of this connector. These outputs are negative true.
5	BCD Bit 400	To Printer	
6	BCD Bit 100	To Printer	
7	BCD Bit 200	To Printer	
8	BCD Bit 40	To Printer	
9	BCD Bit 80	To Printer	
10	BCD Bit 10	To Printer	
11	BCD Bit 20	To Printer	
12	BCD Bit 4	To Printer	
13	BCD Bit 8	To Printer	
14	BCD Bit 2	To Printer	
15	BCD Bit 1	To Printer	
16	BCD Data Autorange Bit 1	To Printer	Negative true BCD coded.
18	BCD Data Autorange Bit 2	To Printer	Autorange Data 00 = No power of 10 01 = BCD output times 10 10 = BCD output times 100 11 = BCD output times 1000 For Total Bits 00 = BCD output times 10^4_5 01 = BCD output times 10^6 10 = BCD output times 10^7 11 = BCD output times 10^7
17	Reset Count	To 3000E	A low input resets all the displays' counters.
19	Sync Recovered	To Printer	Normally high (5V) signal which goes low (0V) when test set recovers sync.
20	Not Used		
21	Signal Ground		
22	Not Used		
23	Not Used		

TABLE 2-6. IDS PRINTER INTERFACE DESCRIPTION (continued)

Pin Number	Signal Name	Signal Flow	Description
24	Sync Lost	To Printer	Normally high (5V) signal to indicate that test set is in sync. This signal goes low when the Model 3000E is out of sync.
25	Frame Ground		
26	Errored Seconds Select	To 3000E	A high requests Errored Second BCD Data at output connector.
27	Total Seconds Select	To 3000E	A high requests Total Bits BCD Data at output connector.
28	Errored Bits Select	To 3000E	A high requests Errored Bits BCD Data at output connector.
29	Not Used		
30	Receive Data (RD)	To Printer	Normally high, goes low if no RD is detected.
31	Clear to Send (CTS)	To Printer	Normally high, goes low if no CTS is detected.
32	Data Set Ready (DSR)	To Printer	Normally high, goes low if no CTS is detected.
33	Serial Clock Transmit (SCT)	To Printer	Normally low, goes high if no SCT is detected.
34	Signal Quality/Automatic Gain Control (SQ/AGC)	To Printer	Normally low, goes high if no SQ/AGC is detected.
35	Ring Indicator (RI)	To Printer	Normally low, goes high if no RI is detected.
36	Data Carrier Detect (DCD)	To Printer	Normally high, goes low if no DCD is detected.
37	Not Used		

2.7 Strapping

After completing the mechanical and electrical installation, various strap-selectable interface options can be set within the Data Test Set. These straps are accessible by the removal of the top cover. Strapping is accomplished by the positioning of two jumper plugs and the setting of two DIP switches located on the interface board (see Figure 2-4). These options are selectable for the RS-422/423 interface. Figure 2-5 lists these options and illustrates the strapping configurations.

NOTE: If the RS-422/423 interface option is selected for any of the timing and data signals, the center conductor of the "B" BNC for SEND TIMING, RECEIVE TIMING, and RECEIVE DATA must be grounded to the shield of the BNC or to signal ground.

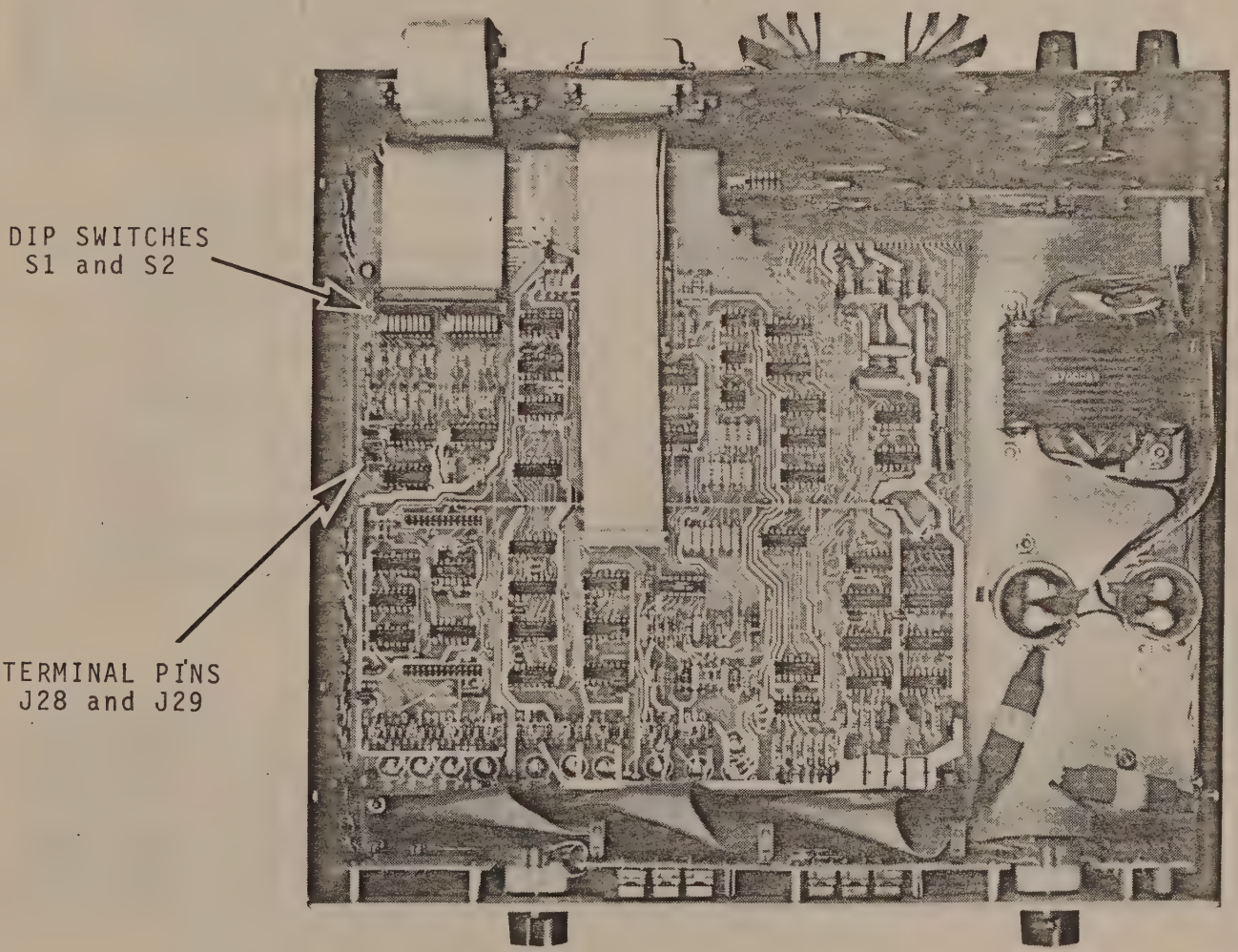
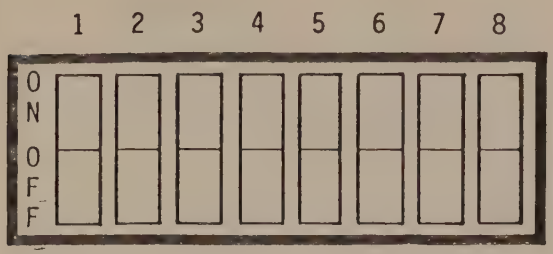
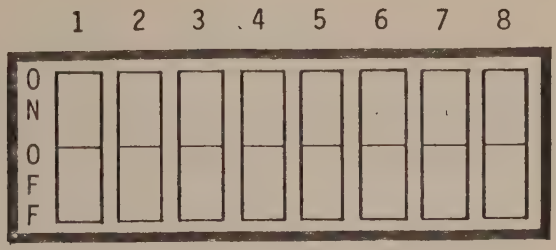


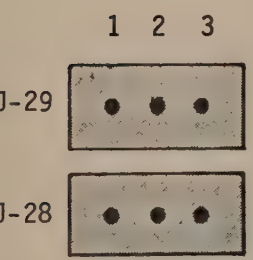
Figure 2-4. Strap Locations





SIGNAL FUNCTION	RS-422	RS-423	TERMINATING RESISTOR*
RECEIVE DATA (RD)	S2-6 OFF	S2-6 ON	S2-5 ON
RECEIVE TIMING (RT)	S2-8 OFF	S2-8 ON	S2-7 ON
SEND TIMING (ST)	S2-2 OFF	S2-2 ON	S2-1 ON
CLEAR TO SEND (CS)	S2-4 OFF	S2-4 ON	S2-3 ON
DATA MODE (DM)	S1-2 OFF	S1-2 ON	S1-1 ON
RECEIVER READY (RR)	S1-4 OFF	S1-4 ON	S1-3 ON

*RS-422 ONLY



SIGNAL FUNCTION	RS-422	RS-423
SEND DATA (SD)	J-29 1 to 2	J-29 2 to 3
TERMINAL TIMING (TT)	J-28 1 to 2	J-28 2 to 3

Figure 2-5. RS-422/423 Interface Options

3.0 OPERATION

3.1 General

This section describes all front panel controls and indicators and provides information on power-up and operation/test procedures. The operator should become familiar with all controls and indicators before attempting to operate the test set.

3.2 Controls and Indicators

Front panel controls and indicators are shown in Figure 3-1 and described in the following paragraphs.

3.2.01 Pattern

This rotary switch selects any one of seven different test patterns, controlling both the transmitter and receiver of the test set. The switch allows the user to select the desired pseudo-random pattern; the alternate mark-space pattern; or steady mark or steady space.

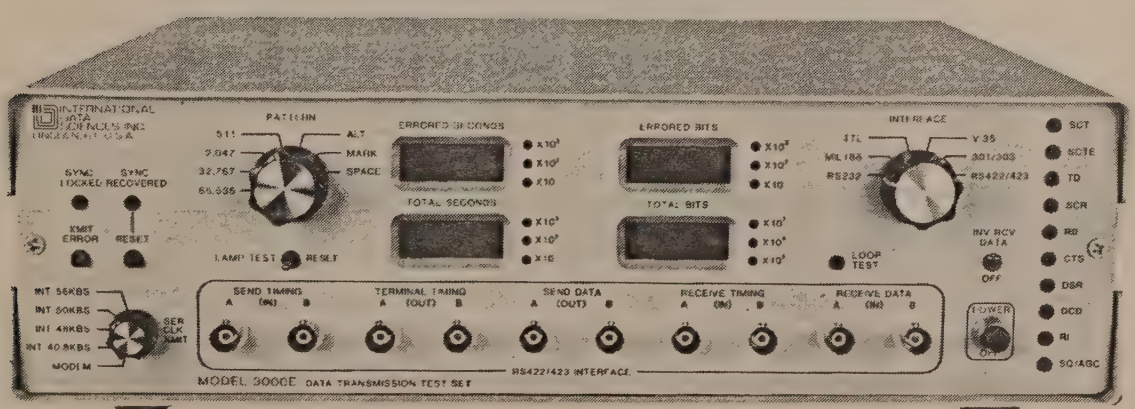


Figure 3-1. Front Panel Controls and Indicators

3.2.02 Counters

The Data Test Set's counters are divided into four displays: Errored Seconds, Total Seconds, Errored Bits, and Total Bits. Each display contains a three digit counter and three LED indicators. The three LEDs are used to indicate the power of ten by which the displayed number is to be multiplied. No LED indicates that the number displayed is to be multiplied by 10^0, the remaining multipliers are marked accordingly. In the case of the Total Bits display, no LEDs indicate " x 10^4", all other multipliers are marked accordingly. Counter overflow is indicated by a flashing display.

3.2.03 Lamp Test/Reset

This three-position toggle switch resets the counter displays and data analyzer. If the switch is held in the Lamp Test position, all LEDs and all counter displays are lit for inspection. In both Reset and Lamp Test positions, this switch is momentary.

3.2.04 Interface

This six-position rotary switch selects any one of the six interfaces standard in the Data Test Set.

3.2.05 Loop Test

This LED is lit whenever the rear panel loop test plug is inserted into any of the 25-pin interface connectors.

3.2.06 INV RCV DATA

This two-position toggle switch inverts the data analyzer's received data. The inversion takes place after the interface circuits; therefore, the RD LED is not affected by this switch.

3.2.07 Channel Monitor LEDs

These ten LEDs along the right side of the front panel monitor the Mark/Space status of key signals of the selected interface. The LEDs used and the polarity of the indicators vary between interfaces. Table 3-1 shows the LEDs used and the status of the signal line when the LED is lit.

TABLE 3-1. MONITOR LEDS

	SCT	SCTE	TD	SCR	RD	CTS	DSR	DCD	RI	SQ/AGC
RS-232	SP	SP	SP	SP	SP	ON	ON	ON	ON	ON
MIL-188	MK	MK	SP	MK	SP	ON	ON	ON	ON	ON
TTL	MK	MK	SP	MK	MK	NA	NA	NA	NA	NA
V.35	SP	SP	SP	SP	SP	ON	ON	ON	ON	NA
301/303	SP	SP	SP	SP	SP	ON	ON	NA	ON	ON
RS/422	SP	SP	SP	SP	SP	ON	ON	ON	ON	ON
RS/423	SP	SP	SP	SP	SP	ON	ON	ON	ON	ON

MK - Indicates a Mark status will light the LED.
SP - Indicates a Space status will light the LED.
NA - Indicates the LED does not apply for that interface and shall remain off.
ON - Indicates a control On status will light the LED.

3.2.08 Sync Locked

This LED indicates that the receiver is operating properly and that it is in sync with the incoming data.

3.2.09 Sync Recovered

This LED indicates that the receiver has lost and subsequently regained sync.

3.2.10 XMIT Error

This pushbutton switch is used to confirm proper operation of the Data Test Set as well as its entire configuration. One error is transmitted for every depression of the switch. If the Data Test Set and the system are working properly, the Errored Bits counter will increment every time the XMIT Error switch is depressed.

3.2.11 Sync Recovered Reset

This pushbutton switch will reset the Sync Recovered LED on the front panel.

3.2.12 Serial Clock XMIT

This five-position rotary switch selects any of the four internal transmitter clocks or the clock generated by the modem in the system.

When the external clock is selected, the internal clocks are bypassed. The incoming transmitter clock is regenerated to become an external transmitter clock at the interface. The same transmitter clock is used to generate the pseudo-random and alternate patterns for transmit data. Receive clock is used to operate the data analyzer and sync detect circuits. Minimum and maximum data rates as a function of cable length and interface are described in Table 3-2.

3.2.13 Power-Up

This pushbutton switch controls the AC power input.

CAUTION: Before attempting to power-up the Data Test Set, assure that it has been switched to the proper line voltage!

TABLE 3-2. MAXIMUM AND MINIMUM DATA RATES

INTERFACE	CABLE LENGTH IN FEET	MAXIMUM	MINIMUM WITH PRINTER	MINIMUM WITHOUT PRINTER
RS-422	50	10 Mbs	25 Bps	1 Bbs
TTL	1	10 Mbs	25 Bps	1 Bps
301/303	50	5 Mbs	25 Bps	1 Bps
V.35	50	3 Mbs	25 Bps	1 Bps
MIL-188	50	1 Mbs	25 Bps	1 Bps
RS-423	50	200 Kbs	25 Bps	1 Bps
RS-232	50	200 Kbs	25 Bps	1 Bps

3.3 Self-Test

The Model 3000E can be self-tested in all interface modes except RS-422/423 simply by plugging the loop test plug into the desired interface. The Model 3000E should be disconnected from the communication equipment during loop test. When in the loop test configuration, the following test procedure can be used to determine proper operation of the Data Test Set.

3.3.01 a) Insert Loop Back Plug into EIA RS-232 input on rear panel.

b) Set the front panel switches to the following positions:

a) Ser Clk Xmit - Int 56 Kbs
b) Pattern - 65,535
c) Interface - RS-232
d) Inv Data - Off
e) Power - Off

3.3.02 a) Set Power Switch On.

b) Actuate Lamp Test toggle switch.

NOTE: All front panel lamps and all display segments are on.

3.3.03 Release Lamp Test toggle switch.

NOTE: a) In RS-232 and MIL-188 modes, Sync Locked, Loop Test, and all Channel Monitor lamps on extreme right hand side are on. In V.35 mode, SQ/AGC is off. In TTL mode; CTS, DSR, DCD, RI, and SQ/AGC are off. In 303 mode, DCD is off.

b) Total seconds counter is advancing.

c) Total Bits counter is advancing.

3.3.04 Depress and release Xmit Error Switch (not more than once every two seconds).

NOTE: The Errored Seconds and Errored Bits displays are advanced by one each time this switch is actuated.

3.3.05 Hold Reset switch down.

NOTE: All display counters are reset to Ø.

3.3.06 Set Pattern Switch to 32,767.

NOTE: a) Sync Locked Lamp is on.
b) Sync Recovered Lamp is on.

3.3.07 Depress and release Reset Sync Recovered.

NOTE: Sync Recovered Lamp is off.

3.3.08 Set Pattern Switch to 2047.

NOTE: Sync Locked Lamp is on.

3.3.09 Set Pattern Switch to 511.

NOTE: Sync Locked Lamp is on.

3.3.10 Set Pattern Switch to ALT.

NOTE: Sync Locked Lamp is off.

3.3.11 Set Pattern Switch to Mark.

NOTE: TD Lamp is off.

3.3.12 Set Pattern Switch to Space.

NOTE: TD Lamp is on.

3.3 Self-Test (continued)

This Self-Test can be used on each interface simply by selecting the desired interface on the front panel and inserting the Loop Back connector into the appropriate input receptacle. The Loop Back connector is not used to test the RS-422/423 interface.

To test this interface, it is necessary to leave the Loop Back connector in its storage location and to use the front panel BNC for Self-Test loop around.

NOTE: First set DIP switches and J28 and J29 terminal pins to the RS-422 setting. Terminating resistors are not necessary.

Connect Ser Clk Xmit Ext (out) A & B to Ser Clk Xmit (in) and Ser Clk Rcv (in) A & B, respectively. Connect Xmit Data (out) A & B to Rcv Data (in) A & B; the RS-422/423 interface can now be tested using the test procedure previously described.

4.0 OPTIONS

4.1 Clock Rate

The Data Test Set has four internally generated clocks and is capable of accepting an external clock from a modem. Two of the internally generated clocks (40.8 and 48 Kbps) may be substituted by a clock rate required by the user.

In order to achieve the optional data rate, the correct crystal frequency must be calculated and the "divide by N" counters in the circuit must be programmed. Programming the counters is achieved by strapping the "E" points provided on the A3 (Interface) Board within the Data Test Set. Crystal selection and strapping will have to be performed at the factory. It is not recommended to modify the Data Test Set in the field.

4.2 Rack Mount

An optional rack mount adapter is available for mounting the Data Test Set in a standard 19-inch cabinet (see Figure 4-1). This option consists of a window-frame type front panel measuring 5¼ inches high by 19 inches wide (13.3 cm H x 48.3 cm W) secured to the unit by side panels. The unit is then mounted in the rack through the front panel by four screws supplied with the option.

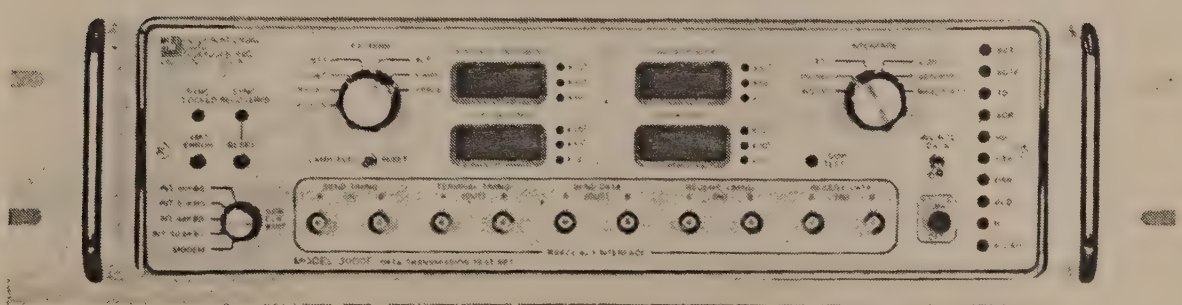


Figure 4-1. Rack Mount Adapter

APPENDIX

MODEL 3000E SPARE PARTS LIST

QTY.	PART NO.	REF. DESIG.	DESCRIPTION	VENDOR	REMARKS
1	PL-370810	A1 Ass'y	P.C. Board Assembly	IDS	
1	PL-370820	A2 Ass'y	P.C. Board Assembly	IDS	
1	PL-370830	A3 Ass'y	P.C. Board Assembly	IDS	
1	PL-370840	A4 Ass'y	P.C. Board Assembly	IDS	
1	PL-370850	A5 Ass'y	P.C. Board Assembly	IDS	
1	PL-370488	49	A.C. Sub Assembly	IDS	
10	6-401-5	BNC 1-10	BNC Connectors	IDS	
1	6-452-1109	S3	Rotary Switch	IDS	
1	6-452-1102	S4	Rotary Switch	IDS	
1	PL-370896-1	74	Ribbon Cable Ass'y: TTL	IDS	
1	PL-370896-2	75	Ribbon Cable Ass'y: RS-232	IDS	
1	PL-370896-3	76	Ribbon Cable Ass'y: V.35	IDS	
1	PL-370896-4	77	Ribbon Cable Ass'y: 301/303	IDS	
1	PL-370897-1	78	Ribbon Cable Ass'y: Printer	IDS	
1	PL-370897-2	79	Ribbon Cable Ass'y: 422/423	IDS	
1	PL-370896-5	80	Ribbon Cable Ass'y: MIL-188	IDS	
1	PL-370307	86	Plug Storage Assembly	IDS	
1	6-290-7	F1	3/4A, SB Fuse	IDS	
1	6-290-208815	F2	3/8A, SB Fuse	IDS	
1	6-432-600001	P27	A.C. Line Cord	IDS	

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CALIBRATION AND REPAIR SERVICE

All units sold by International Data Sciences, Inc. are calibrated at the time of delivery. International Data Sciences, Inc. recommends a periodic calibration every six months thereafter performed by the Calibration Department at International Data Sciences, Inc. Contact IDS for the cost of each calibration. If the unit requires repairs that are not covered by the original warranty, then IDS will perform the repair at an hourly charge plus parts. Normal turn-around time for calibration is two weeks.

Equipment so calibrated will bear a gummed label on the rear panel identifying the serial number of unit calibrated; the date of calibration; the next recommended calibration date; and the in-plant calibrator identifier.

All units returned to IDS for calibration will be accepted only if transportation charges are prepaid. The purchaser is also responsible for all transportation charges incurred in returning the calibrated unit to the purchaser.

For fast service, Federal or Emery Air Freight are recommended. If time is not a problem, UPS is recommended. Return address should be clearly stated and should include a person to the attention of whom unit will be shipped.

Shipping cartons with proper foam packing are available from IDS. The carton will facilitate shipping the equipment to be calibrated with a maximum of protection.

For most expeditious service, when returning the equipment for repair, please fill out the Trouble Report in your manual of operation.

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MODEL 3000E TROUBLE REPORT

1) Please indicate what positions the following switches were in:

PATTERN		INTERFACE		SER CLK XMIT
__ 65,535	__ ALT	__ RS-232	__ V.35	__ INT 56 KBS
__ 32,767	__ MARK	__ MIL-188	__ 301/303	__ INT 50 KBS
__ 2,047	__ SPACE	__ TTL	__ RS-422/423	__ INT 48 KBS
__ 511				__ INT 40.8 KBS
				__ MODEM

INV RCV DATA
__ ON
__ OFF

2) Please check only the lamps that were on.

__ SYNC LOCKED	__ SCT	__ SCR	__ DSR	__ SQ/AGC
__ SYNC RECOVERED	__ SCTE	__ RD	__ DCD	
__ LOOP TEST	__ TD	__ CTS	__ RI	

ERRORED SECONDS	TOTAL SECONDS	ERRORED BITS	TOTAL BITS
__ $X10^3$ __ X10	__ $X10^3$ __X10	__ $X10^3$ __ X10	__ $X10^7$ __ $X10^5$
__ $X10^2$	__ $X10^2$	__ $X10^2$	__ $X10^6$

3) Please draw or give a description of how the test set was being used. Describe connector used, equipment type, and malfunction of test set or system. (Use back of page if additional room is needed.)

4) Please give name, address, and telephone number of the person to contact about this unit.

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